What is claimed is:

1. A processor including an operation instruction comprising an instruction code and at least one register designating field, wherein the at least one register designating field is capable of designating a plurality of registers having consecutive numbers.

2. A processor comprising:

a decoder designating a plurality of read registers in one field in an arbitrary number of register designating fields; and

a register file for outputting data in a plurality of registers having consecutive numbers in accordance with an output from the decoder.

3. A processor comprising:

a decoder for designating a plurality of write registers in one field in an arbitrary number of register designating fields; and

a register file capable of writing values in a plurality of registers having consecutive numbers in accordance with an output from the decoder.

4. The processor according to Claim 2,

wherein the register file includes a plurality of banks, and by reading or writing data from the plurality of banks, the number of ports of reading or writing the data of the respective banks is restricted to be equal to or

smaller than the number of the register designating fields, to thereby restrain an increase in a circuit scale caused by reading or writing the data by a number of times larger than the number of the fields.

5. The processor according to Claim 1,

wherein the number of the plurality of registers having the consecutive number is limited to the n-th power of 2 (n is a natural number), to thereby enable to reduce register selecting circuits.

6. The processor according to Claim 1,

wherein a data pack operation, which is capable of dealing with a number of the data read from the read registers larger than a number of the data written to the write registers in order to read data from the registers larger in a number than the number of the read register designating fields, is realized without producing invalid portions in the write registers.

7. The processor according to Claim 1,

wherein a data unpack operation, which is capable of dealing with a number of the data written to the write registers larger than a number of the data read from the read registers such that the data can be written to the registers larger in a number than the number of the write register designating fields, is realized in parallel without executing data writing a plurality of times.

8. The processor according to Claim 1,

wherein an operation of outputting the data having a data width wider than a width of input data such that the data can be written to the registers larger in a number than the number of the write register designating fields, is realized without producing an invalid portion in the input data and without mounting a special register having a wider data width.